REMARKS

The Official Action mailed November 22, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to March 24, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on July 17, 1998, March 21, 2000, April 25, 2000, July 17, 2000, November 30, 2000, March 9, 2001, April 11, 2001 and November 2, 2001.

Claims 1-8 and 11-73 are now pending in the present application, of which claims 1, 5, 11, 12, 18, 23, 28, 33, 38, 40, 43, 47, 53, 59, 64 and 69 are independent. Applicant notes with appreciation the allowance of claims 1-8 and 11-46. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action rejects claims 47-73 as obvious based on the combination of U.S. Patent No. 5,055,899 to Wakai et al. and U.S. Patent No. 5,427,961 to Takenouchi et al. In a telephone conversation between the Applicants' representative and the Examiner, it was understood that the recitation of two substrates (i.e. first and second resinous substrates) is allowable subject matter. In response, independent claims 47, 53, 59, 64 and 69 have been amended to recite "a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate." Wakai and Takenouchi, either alone or in combination, do not teach a second resinous substrate which is opposed to a first resinous substrate. Since Wakai and Takenouchi do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained, and the Applicants respectfully submit that claims 47-73 are in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

47. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film interposed therebetween.

48. (Amended) The device of claim 47 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

53. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region between said source region and said drain region; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

54. (Amended) The device of claim 53 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

59. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film interposed therebetween.

64. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

69. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.